CHAPTER 1:
OPERATIONAL AMPLIFIER

1. PURPOSE. This method establishes the means for measuring input offset voltage and current, input bias current, common mode rejection ratio, supply voltage rejection ratio, voltage gain, output voltage swing, input offset voltage adjustment range, power supply current, output short circuit current, channel separation, rise time, slew rate, broadband noise, popcorn noise, noise voltage density, noise current density, overshoot and settling time for operational amplifiers.

2. DEFINITIONS. The following definitions apply for the purpose of this test method.

2.1 Input Offset Voltage (V_{IO}). Input offset voltage is the dc voltage which must be applied between the input terminals through two equal resistances to force the quiescient dc output to zero or other specified level.

2.2 Input Offset Voltage Temperature Sensitivity (ΔV_{IO}). Input offset voltage drift is the ratio of the change of input offset voltage ΔV_{IO} to the change of circuit temperature (ΔT). This typically generates a value expressed as microvolts per degree (°C).

2.3 Input Offset Voltage Adjustment Range ($V_{IO}(adj+)$, $V_{IO}(adj-)$). The input offset voltage adjustment ranges are the differences between the offset voltage (V_{IO}) measured with the voltage adjust terminals open circuited, and the offset voltage measured with the maximum positive or negative voltage attainable with the specified adjustment circuit.

2.4 Input Bias Current ($+I_{IB}$, $-I_{IB}$). The input bias currents are the currents flowing into the inverting (-) and non-inverting (+) terminals of an operational amplifier.

2.5 Input Offset Current (I_{IO}). The input offset current is the algebraic difference between the currents entering into the input terminals of a differential input amplifier.

$$I_{IO} = (+I_{IB}) - (-I_{IB})$$

2.6 Input Offset Current Temperature Sensitivity (ΔI_{IO}). Input offset current drift is the ratio of the change in input offset current (ΔI_{IO}) to the change of circuit temperature (ΔT). This typically generates a value expressed as picoamps per degree (°C).

2.7 Common Mode Input Voltage Range (V_{CM}). This is the range of common mode input voltage over which proper function of the operational amplifier is maintained. This parameter is guaranteed by testing CMRR to the limits of V_{CM}.

2.8 Common Mode Rejection Ratio (CMRR). The common mode rejection ratio is the ratio of the change in input common mode voltage to the resulting change in the input offset voltage. CMRR is usually expressed in decibels:

$$\mathrm{CMRR} = 20\ \mathrm{LOG}\left(\frac{\Delta V_{CM}}{\Delta V_{IO}}\right)$$

where

ΔV_{IO} = change in input offset voltage

ΔV_{CM} = change in common mode input voltage

2.9 Power Supply Rejection Ratio (PSRR). The power supply rejection ratio is the ratio of the change in input offset voltage, V_{IO}, to the corresponding change in power supply voltage usually expressed in microvolts per volt. PSRR may be tested either by shifting the voltage of one power supply with all remaining power supply voltages held constant, or by shifting both power supply voltages simultaneously. For the first method +PSSR and -PSSR are defined as follows:

$$+\mathrm{PSSR} = \frac{\Delta V_{IO}}{\Delta(+V_{CC})} \qquad -V_{CC} = \text{constant}$$

$$-\mathrm{PSRR} = \frac{\Delta V_{IO}}{\Delta(-V_{CC})} \qquad +V_{CC} = \text{constant}$$

For the second method, PSRR is defined as:

$$\mathrm{PSRR} = \frac{\Delta V_{IO}}{\Delta(V_{CC})}$$

where

ΔV_{CC} is obtained by shifting both power supplies, for example, from ±20 V to ±5 V.

2.10 Power Supply Current (ICC). Power supply currents are the currents flowing into the positive and negative supply terminals of the operational amplifier.

2.11 Voltage Gain (A_V). The voltage gain (open loop) is the ratio of the change in the output voltage to the differential change in the input voltage. The input not connected to the signal source is at zero potential.

2.12 Output Voltage Swing (VOP). The maximum output voltage swing that can be achieved for a specified load without causing voltage limiting.

2.13 Channel Separation. This parameter is specified for dual and quad operational amplifiers integrated on the same semiconductor chip. It is a measure of the amount of electrical coupling between amplifiers. When a signal is applied at the input of one amplifier, some portion will appear at the output of the other amplifier or amplifiers. Channel separation is measured in decibels.

2.14 Rise Time (t_R). The rise time of an operational amplifier is the time necessary for the output of the amplifier to rise from 10% of its output steady state value to 90% of its output steady state value for a specified input pulse.

2.15 Settling Time (t_s). The settling time for an operational amplifier is the time required for the amplifier output to change from some specified voltage level and to settle within a specified errorband of its final steady state value in response to the application of a specified input pulse.

2.16 Slew Rate (SR). Slew rate is defined as the maximum rate of change of output voltage per unit of time and is expressed in volts per microsecond.

2.17 Broadband Noise ($N_{I(BB)}$). Broadband noise referenced to the input is the true rms noise voltage including all frequency components measured at the output of the amplifier. Practical measurement of broadband noise requires specification of a minimum bandwidth over which the output noise voltage is measured.

2.18 Popcorn Noise ($N_{I(PC)}$). Popcorn noise consists of randomly occurring bursts of noise across the broadband range. $N_{I(PC)}$ is expressed in mV peak referenced to the amplifier input.

2.19 Input Noise Voltage Density (E_n). The input noise voltage density is the rms noise voltage in a 1 Hz band centered on a specified frequency.

E_n is typically expressed in $nV/\sqrt{Hz}$ referenced to the amplifier input.

2.20 Input Noise Current Density (I_n). The input noise current density is the rms noise current in a 1 Hz band centered on a specified frequency.

I_n is typically expressed in $nA/\sqrt{Hz}$ referenced to the amplifier input.

2.21 Transient Response Overshoot (O_s). Overshoot is measuring using the test circuit shown in Figure 5. An input pulse of rise time and amplitude as specified in the procurement document is applied to the amplifier and the output waveform is observed on the oscilloscope. Pulse duration and repetition rate are set to enable easy observation of the output waveform. The overshoot is determined as the maximum amount of the voltage swing above V2. The value V2 is the final output voltage that is obtained when the device has fully settled

2.22 Low Frequency Input Noise Density (E_{npp}). Low frequency input noise density is the peak to peak noise voltage in the frequency range of 0.1 Hz to 10 Hz.

2.23 Unity-Gain Bandwidth. Defined as the frequency at which the open-loop voltage gain is unity. (Gain Bandwidth and Gain Bandwidth Product are other terms which also express the useful frequency range of an amplifier). This parameter is difficult to measure directly in a production environment. Transient response rise time and slow rate are more typically measured to evaluate the frequency response of an operational amplifier.

3. APPARATUS. The apparatus shall include the necessary equipment needed to implement the test circuits shown in Figures 1, 2, 4, 5, 7 and 8. If the optional integrated capacitor method is used to measure leakage currents, then additional circuit components needed to implement the setup in Figure 3 may be required. Operational amplifier bias power supplies not shown in the figures will be as specified in the procurement document.

3.1 DC Voltmeters (VM1, VM2). The dc voltmeters shown in Figures 1, 2 and 3 shall have input impedances sufficiently high as not to load the circuit under test. Accuracy shall be such that it will have less than ten percent effect on the tolerance specified for the circuit tested. For example, if a reading should be 0 ± 0.1V to be acceptable for the circuit tested, the voltmeter shall be accurate to within ±0.01 V.

3.2 DC Current Meters (CM1, CM2). Current meters are required to measure the supply currents of the device and output short circuit current. The current meters should be accurate to 0.1% over the range of current to be measured. Additionally, the current meter used to measure the short circuit output current must be programmable to make measurements at a specified time following the application of the short circuit voltage condition at the voltage output pin.

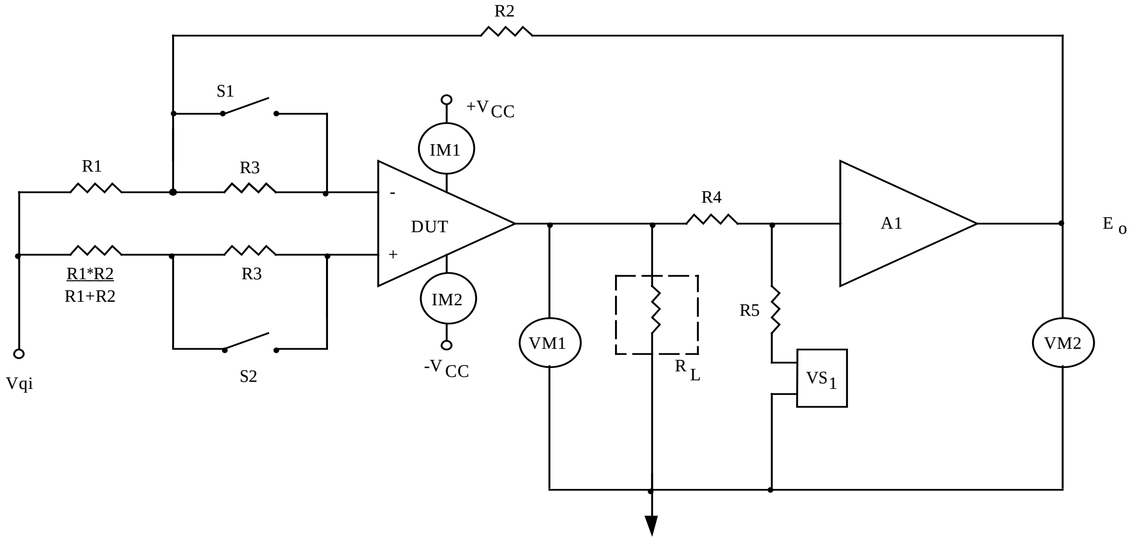
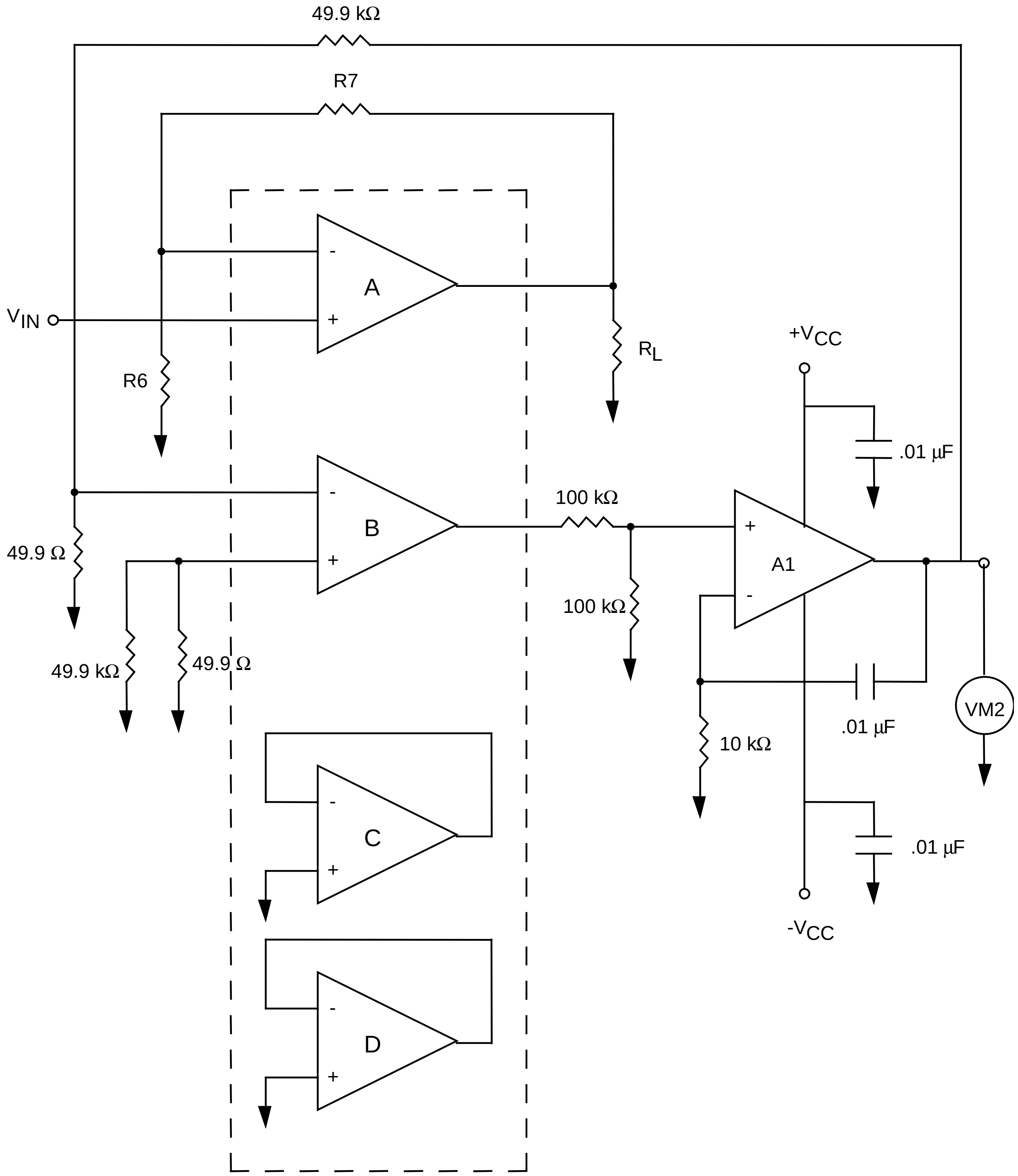


Figure 1: Operational Amplifier Test Circuit

3.3 Bias Power Supplies. Device power supplies will be programmable to provide $+V_{CC}$ and $-V_{CC}$ voltages at nominal levels specified for the device in test. The supplies shall be accurate to 0.1%.

3.4 Stabilization Networks. For all test circuits, stabilization shall be appropriate to stabilize the circuit to prevent oscillation. If a maximum peak-to-peak level of oscillation is specified in the procurement document, then an oscillation detector at the device output shall be used to guarantee that peak-to-peak noise above this level shall be cause for device failure.

3.5 Resistor and Capacitor Networks. The value of the resistors not specified in the appropriate test circuit will be provided by the procurement document. Alternatively, in Figure 1, resistor R_2 shall be chosen to have a value no larger than the nominal input



Notes:
1. All resistors +/- 0.1% tolerance, all capacitors +/- 10% tolerance
2. The nulling amplifier shall be MIL-M-38510/135 or similar. Saturation of the amplifier is not allowed

Figure 2: Channel Separation Test Circuit

impedance nor less than a value which will load the amplifier (10*Z_o). R_1 should be chosen such that $R_2 / R_1 = 1000$ or some other convenient scale factor. Resistors used for setting loop gain shall be within 0.1% or better precision. All other resistors shall be within 1% of the specified value. The accuracy of the capacitors used in all test circuits (except Figure 3) shall be ±10% unless otherwise specified in the procurement document.

3.6 Operational Amplifier. The nulling operational amplifier, A1, in Figures 1, 2 and 3 amplifies and inverts error voltages at the output of the DUT. Recommend precision operational amplifier with lower offset then the DUT as a minimum the nulling amplifier should have an offset of less than 10% of that of the DUT.

3.7 Output Voltage Supply (VS_1). The output voltage supply in Figure 1 will be programmable to force a specific output voltage on the amplifier under test. The supply must have an accuracy of 0.01%.

3.8 Programmable Load Resistor (R_L). The load resistor in Figures 1 and 2 must be programmable or switch selectable to simulate any load required for the amplifier under test. The values needed will be obtained from the procurement document and may include an open circuit condition. Resistors will be accurate to within 1.0%.

3.9 Integrating Capacitor. The integrating capacitor used in the low leakage test circuit shown in Figure 3 must have a dielectric resistance sufficiently high as to contribute less than 10% to measured leakage. In addition the capacitor should have low dielectric absorption.

3.10 Pulse Generator (VS_2). The pulse generator used in Figures 4 and 5 shall have a rise time and repetition rate sufficient to perform the tests described in Sections 4.16 to 4.18 on the amplifier under test. The pulse generator must also have an output impedance of 50Ω.

3.11 Pulse Shaping Network. Some test circuits may require an RC network between the pulse generator and the amplifier under test for matching purposes as shown in Figures 4 and 5. This network must be specified in the procurement document.

3.12 Oscilloscope (OSC). The oscilloscope or alternate time measuring system shown in Figures 4 and 5 shall have sufficient bandwidth to measure timing parameters equivalent to those in the specification with an accuracy of 1%. The oscilloscope shall have an input impedance of 1 MΩ or greater. Some device types may require the use of a FET probe or other high impedance buffer device to minimize distortion of output waveform.

3.13 AC Voltmeter (VM3). An ac voltmeter is required to make noise measurements using the circuit in Figure 7. For broadband noise VM3 must read true rms voltage.

Popcorn noise requires a peak reading voltmeter or equivalent apparatus. VM3 must have a minimum bandwidth of 10 Hz to 15 KHz.

3.14 Noise Analyzer Amplifier and Filter Units. The test circuit in Figure 8 requires both an amplifier and filter unit. The characteristics of these units are described in more detail in Sections 4.21 and 4.22.

3.15 Input Voltage (V_{qi}). The voltage supply used in Figure 1, controls the DUT input voltage.

4. PROCEDURE. The approach used to measure operational amplifier static parameters is the nulling amplifier method illustrated in Figure 1. An alternative approach, the integrating capacitor method, shown in Figure 3, is also described for measurement of very low currents. Table 1 summarizes the test conditions, measurements and equations for all static tests. Circuits and diagrams needed to measure the dynamic performance of operational amplifiers are shown in Figures 4 to 8. Dynamic parameters are measured using the test circuits shown in Figures 4 and 5. Figures 7 and 8 show test circuits used to measure the noise characteristics of the amplifier under test. The test conditions, measurements and equations for these parameters are included on the test circuit diagrams and in the following text instead of Table 1.

4.1 Input Offset Voltage (V_{IO}). Input offset voltage is tested with switches S_1 and S_2 closed. V_{S1} is set to required condition. The nulling amplifier output, E_o is measured and V_{IO} determined from the equation:

$$V_{IO} = \left(\frac{R_1}{R_2} - 1\right) E_o \qquad \mu V$$

4.2 Input Offset Voltage Adjustment Range ($V_{IO}(adj)$). The input offset voltage adjust is determined by measuring input offset voltage (V_{IO}) using the procedure in Section 3.1. Maximum positive and negative adjust ranges are measured. Maximum applied voltages at the adjust terminals will be specified in the procurement document. Two values are measured. $V_{IO}(+)$ is determined by measuring with the maximum condition applied to the positive adjust terminal. $V_{IO}(-)$ is found similarly except the maximum is applied to the negative terminal. Then:

$$V_{IO}(adj+) = V_{IO} - V_{IO}(+) \qquad V$$

$$V_{IO}(adj-) = V_{IO} - V_{IO}(-) \qquad V$$

where

V_{IO} is the input offset voltage measured in Section 4.1.

Table 1: Equations for Static Operational Amplifier Tests

Parameter	Switches		Load Resistor R_L	Output Voltage vs_1	Measurement		Equation	Unit	Notes
	S_1	S_2							
V_{IO}	Closed	Closed	Open	A_D	VM2	E_0	$V_{IO} = (E_o) / A_D$	Volt	Figure 1 See Note 1
V_{IO} (adj)	Closed	Closed	Open	A_D	VM2	E_1	$V_{IO}(adj+) = (E_o - E_1) / A_D$	Volt	Figure 1
	Closed	Closed	Open		VM2	E_2	$V_{IO}(adj-) = (E_o - E_2) / A_D$	Volt	See Note 2
I_{IO}	Closed	Closed	Open	A_D	VM2	E_3	$I_{IO} = \frac{R_1}{R_2}\left(\frac{E_3 - E_4}{R_3}\right)$	Amps	Figure 1
	Open	Open	Open	A_D	VM2	E_4			See Note 1
I_{IB}	Closed	Open	Open	A_D	VM2	E_5	$+I_{IB} = \left(\frac{R_1}{R_2} + 1\right)\left(\frac{E_5 - E_o}{R_3}\right)$	Amps	Figure 1
	Open	Closed	Open	A_D	VM2	E_6	$-I_{IB} = \left(\frac{R_1}{R_2} + 1\right)\left(\frac{E_o - E_6}{R_3}\right)$		See Note 1
A_V	Closed	Closed	R_L	V_{o1}	VM2	E_7	$A_V = \left(\frac{V_{o2} - V_{01}}{\Delta E}\right)$	None	Figure 1
	Closed	Closed	R_L	V_{o2}	VM2	E_8	$\Delta E = \frac{E_8 - E_7}{(R_2 / R_1)}$		
VOP	Closed	Closed	R_L	V_{o3}	VM1	E_9	$+VOP = E_9$	Volt	Figure 1
	Closed	Closed	R_L	V_{o4}	VM1	E_{10}	$-VOP = E_{10}$		
CMRR	Closed	Closed	Open	V_{o5}	VM2	E_{11}	$CMRR = 20 * LOG\left(\frac{V_{o6} - V_{o5}}{\Delta E}\right)$	dB	Figure 1
	Closed	Closed	Open	V_{o6}	VM2	E_{12}	$\Delta E = \frac{E_{12} - E_{11}}{(R_2 / R_1)}$		

Table 1: Equations for Static Operational Amplifier Tests (Cont'd)

Parameter	Switches		Load Resistor R_L	Output Voltage vs_1	Measurement		Equation	Unit	Notes
	S_1	S_2							
+PSRR	Closed	Closed	Open	A_D	VM2	E_{13}	$PSSR = \frac{E_{14} - E_{13}}{(R_2 / R_1) * \Delta VCC}$	$\frac{\mu V}{V}$	Figure 1
	Closed	Closed	Open	A_D	VM2	E_{14}			See Note 3
-PSRR	Closed	Closed	Open	A_D	VM2	E_{15}	$PSSR = \frac{E_{14} - E_{13}}{(R_2 / R_1) * \Delta VCC}$	$\frac{\mu V}{V}$	Figure 1
	Closed	Closed	Open	A_D	VM2	E_{16}			See Note 4
+ICC	Closed	Closed	Open		IM1	I1	$+I_{CC} = I_1$	Amps	Figure 1
CS	----	----	R_L	----	VM2	E_{17}	$CS = 20 * LOG \left(\frac{(\Delta V_{IN}) * (R_2 / R_1)}{(E_{18} - E_{17}) / A_L}\right)$	dB	See Fig. 2
	----	----		----		E_{18}			See Note 5

NOTES:

1. If using Integrated Capacitor Method, refer to equations in Section 4.7.
2. E_1 measured with maximum voltage applied to adjust terminal, E_2 measured with minimum voltage applied to adjust terminal.
3. E_{13} measured with $+V_{CC}$ at nominal level, E_{14} measured with $+V_{CC}$ at adjusted level.
4. E_{15} measured with $-V_{CC}$ at nominal level, E_{16} measured with $-V_{CC}$ at adjusted level.
5. A_L is loop gain for nulling amplifier in Figure 2.
6. Input Voltage (V_{qi}) for each test will be specified in the procurement document.
7. $A_D = (R_2 / R_1) - 1$. Loop gain for the circuit in Figure 1.

4.3 Input Offset Voltage Temperature Sensitivity (ΔV_{IO}). Measurement of V_{IO1} is made at temperature T1 as described in Section 4.1, and a second measurement of V_{IO2} is made at the second temperature (T2). ΔV_{IO} is then calculated as:

$$\Delta V_{IO} = \frac{V_{IO2} - V_{IO1}}{T_2 - T_1} \qquad \mu V / °C$$

4.4 Input Offset Current (I_{IO}). The test circuit is initially configured with the load resistor removed, VS_1 programmed to required conditions, and switches S_1 and S_2 both closed. VM2 is used to measure the output voltage, E_3. Switches S_1 and S_2 are then both opened and output voltage E_4 is measured. DI_{IO} is then calculated using the following equation:

$$I_{IO} = \frac{R_1}{R_2}\left(\frac{E_3 - E_4}{R_3}\right) \qquad \mu A$$

4.5 Input Offset Current Temperature Sensitivity (ΔI_{IO}). Measurement of I_{IO1} is made at temperature T_1 and I_{IO2} at temperature T_2 as in Section 4.4. ΔI_{IO} is then calculated as:

$$\Delta I_{IO} = \frac{I_{IO2} - I_{IO1}}{T_2 - T_1} \qquad \mu A / °C$$

4.6 Input Bias Currents ($+I_{IB}$, $-I_{IB}$). Input bias current is tested with load resistor R_L, and power supply VS_1 programmed to required condition. The nulling amplifier output voltage E_o is first obtained with switches S_1 and S_2 closed. Output voltage E_5 is then measured with switch S_1 closed and S_2 open and output voltage E_6 is measured with switch S_1 open and S_2 closed. The input bias currents are calculated as:

$$+I_{IB} = \left(\frac{E_5 - E_o}{R_3}\right)\left(\frac{R_1}{R_2} + 1\right) \qquad \mu A$$

$$-I_{IB} = \left(\frac{E_o - E_6}{R_3}\right)\left(\frac{R_1}{R_2} + 1\right) \qquad \mu A$$

4.7 Input Bias Current ($+I_{IB}$, $-I_{IB}$) by the Integrating Capacitor Test Method. The integrating capacitor method may be used for the measurement of very low input bias currents. Two alternative approaches to the integrating capacitor method are shown in the test circuits of Figures 3(a) and 3(b). Both approaches rely on the basic relationship of the current to the rate of change of voltage when a capacitor is charged by a constant current:

$$I = C \frac{\Delta E}{\Delta t} \qquad \mu A$$

where

I = a constant charging current
C = capacitance of capacitor
$\Delta E / \Delta t$ = charging rate

The method defined by the circuit of Figure 3(a) is suitable for measurement of any small current, I_x , which may be sourced or sunk at point A. To measure the input bias current, $+I_{IB}$ or $-I_{IB}$, at the input of an operational amplifier in test, the device is biased at nominal supply levels and operated in open loop condition. The input to be tested is connected to point A in the test circuit and the other input is connected to zero volts. Voltage E_{o1} is measured initially with switch S closed. The switch is then opened and E_{o2} measured after t seconds. Then:

$$I_x = \frac{-(E_{o2} - E_{o1})}{t} * C \qquad \mu A$$

The method of Figure 3(b) is a variation of the nulling amplifier circuit. To obtain $-I_{IB}$, output voltage E_{o1} is measured with switches S_1 and S_2 closed. S_1 is then opened and after t seconds E_{o2} is measured. Then:

$$-I_{IB} = \frac{-(E_{o2} - E_{o1})}{t} * C_1 * (49.9 / R_F)$$

To obtain $+I_{IB}$, E_{o1} , is again measured with the switches closed, switch S_2 is opened and after t seconds E_{o3} is measured. Then:

$$+I_{IB} = \frac{-(E_{o3} - E_{o1})}{t} * C_1 * (49.9 / R_F)$$

Input offset current may be calculated from $+I_{IB}$ and $-I_{IB}$,

$$I_{IO} = +I_{IB} - (-I_{IB})$$

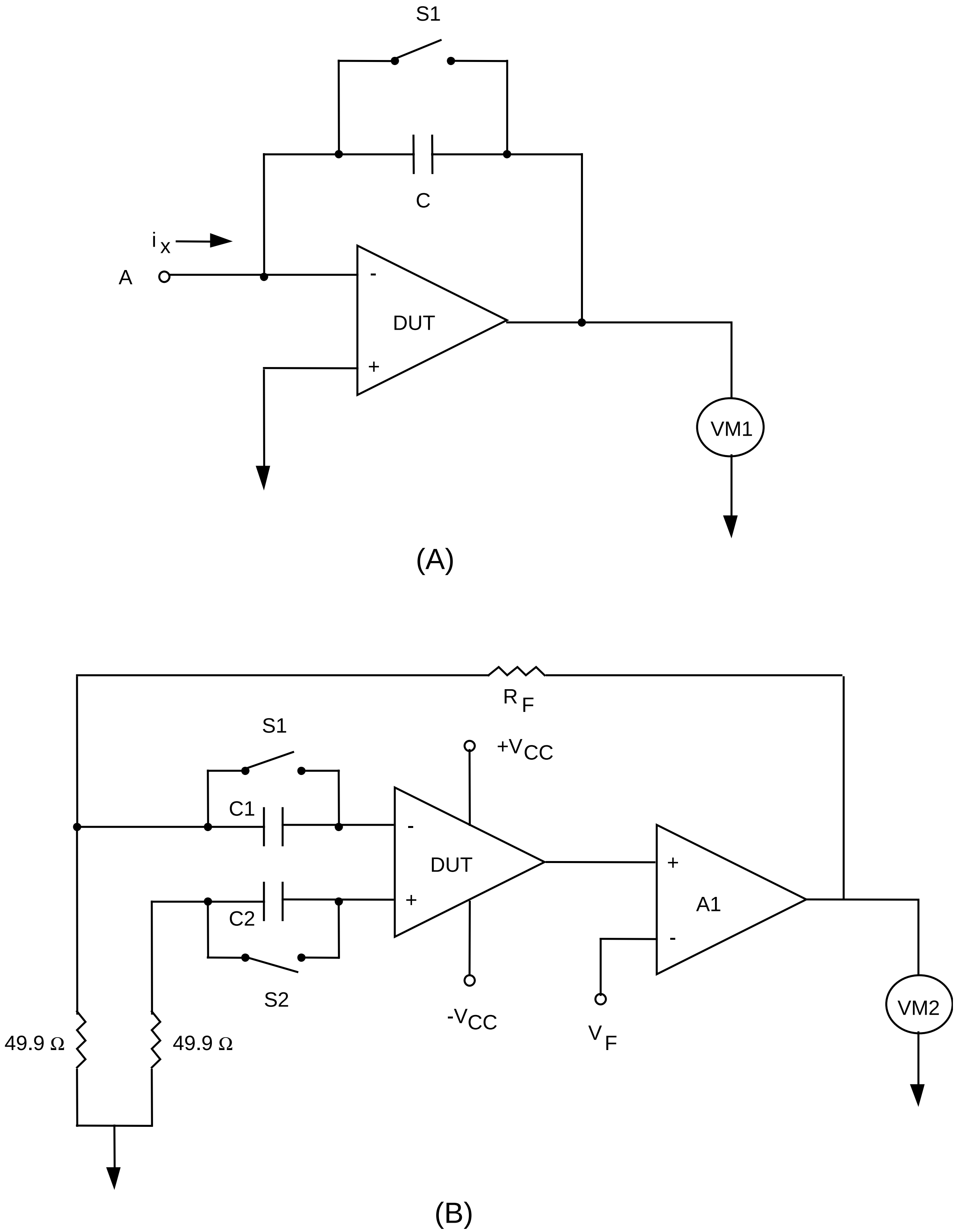


Figure 3: Test Circuits for Low Leakage Current Amplifiers

4.8 Voltage Gain (A_V). Voltage gain of the amplifier is determined by making two measurements with the output voltage and load resistance set as specified in the procurement document. The power supply VS_1 is programmed to the specified output voltage level, V_{O1} and resistor R_L is set to the value specified. VM2 is used to measure voltage E_7 for this condition. VS_1 is then set to the second output voltage level, V_{O2} and E_8 is measured with VM2. The voltage gain is obtained from the equation:

$$A_V = \frac{V_{O2} - V_{O1}}{\Delta E} \qquad V/V$$

where

$$\Delta E = \frac{E_8 - E_7}{(R_2/R_1)}$$

4.9 Output Voltage Swing (VOP). Output voltage swing (peak-to-peak) is tested by driving the output voltage of the amplifier to levels specified in the procurement document. The test determines whether the operational amplifier will reach the specified positive and negative output voltage levels, +VOP and -VOP, for the device. The test is accomplished in the circuit of Figure 1 by driving the input of the nulling amplifier with power supply VS_1 through resistor R_5 set equal to R_4 . The drive levels V_{O3} and V_{O4} will be equal in magnitude and opposite in polarity to the specified operational amplifier outputs. VM1 is used to measure the output voltages, E_9 and E_{10}. Switches S_1 and S_2 are closed for this test. Load resistor R_L is set as specified in the procurement document. The output voltage swing is defined by:

$$+VOP = E_9 \quad \text{and} \quad -VOP = E_{10}$$

4.10 Common Mode Rejection Ratio (CMRR). CMRR is determined from two measurements of the input offset voltage (V_{IO}) with positive and negative common mode voltage (V_{CM}) applied. Common mode conditions are achieved by algebraically subtracting V_{CM} from each supply. For example, if V_{CM} = -11 volts, then $+V_{CC}$ = 15V - (-11V) = +26V and $-V_{CC}$ = -15V - (-11V) = -4V. To center the voltage swing at the input of the nulling amplifier at zero volts, voltage equal to the common mode voltage and opposite in polarity is applied at VS_1 . Let E_{11} be the voltage measured at E_o with VS_1 set at the positive common mode voltage, V_{CM1} , and E_{12} the voltage at E_o with VS_1 set at the negative common mode voltage, V_{CM2} , then:

$$CMRR = 20 * LOG \left(\frac{V_{CM2} - V_{CM1}}{R_1/R_2(E_{12} - E_{11})} \right) \qquad \text{Decibels}$$

4.11 Common Mode Input Voltage Range (V_{CM}). This test shall be an implied measurement. The maximum common mode input voltage specified for the amplifier shall be used in making the common mode rejection ratio test of Section 3.9.

4.12 Power Supply Rejection Ratio (+PSRR, -PSRR). +PSRR and -PSRR are determined by measuring the shift in the input offset voltage occurring when one power supply is shifted from nominal level while the other is maintained at a constant level. This requires two measured values of V_{IO} . These values can be obtained by shifting the power supply once and using the value of V_{IO} obtained under these conditions along with the input offset voltage measured in Section 4.1. Alternatively, the power supply may be shifted above and below the nominal level with V_{IO} measured at each condition. For example, +PSRR may be determined from measurements of V_{IO} made with $+V_{CC}$ at 20V and 10V while $-V_{CC}$ is maintained at -15V. The measured values are scaled to give a result in microvolts change of V_{IO} per volt change in power supply voltage. The equation for +PSRR is:

$$+PSRR = \frac{(R_2/R_1)\,(E_{14} - E_{13})}{\Delta + V_{CC}} \qquad \mu V/V$$

where

ΔV_{CC} = Change in supply voltage
E_{13} = E_o for first $+V_{CC}$ level
E_{14} = E_o for second $+V_{CC}$ level

Similarly,

$$-PSRR = \frac{(R_2/R_1)\,(E_{16} - E_{15})}{\Delta\,(-V_{CC})} \qquad \mu V/V$$

where

ΔV_{CC} = Change in supply voltage
E_{15} = E_o for first $-V_{CC}$ level
E_{16} = E_o for second $-V_{CC}$ level

4.13 Power Supply Current (ICC). The power supply current at each supply will be measured using the current meters CM1 and CM2 (for a device containing dual power supplies).

4.14 Output Short Circuit Current (I_{OS}). Short circuit current will be measured. Two such measurements are required. $I_{OS}(+)$ is measured with the amplifier output at a specified positive voltage, and $I_{OS}(-)$ is measured with a specified negative voltage on the amplifier output. The duration of the short circuit will be specified in the procurement document.

4.15 Channel Separation (CS). Channel separation for dual and quad operational amplifiers is tested in the circuit of Figure 2. CS is tested for each amplifier with respect to all other amplifiers. Thus two tests are performed for a dual amplifier and 12 for a quad operational amplifier. The test circuit of Figure 2 is applicable to both dual and quad amplifiers. The connection shown is for measurement of amplifier B output sensitivity with respect to a signal applied to the input of amplifier A. Amplifiers C and D, if present, are connected as shown for unit gain. The gain setting resistors, R_6 and R_7, for amplifier A will be as specified in the procurement document if required. For many devices, R_6 will be omitted and R_7 will be replaced by a direct connection from the inverting input to the output resulting in a gain of 1 for the driven amplifier.

The test procedure is as follows: Two levels of input voltage V_{IN}, for example, ±10 V, are applied successively and output voltages E_{17} and E_{18} measured by VM2. CS is calculated by comparing the change in output voltage of the driven amplifier with the voltage change at the output of the passive amplifier:

$$CS = 20 * \mathrm{LOG}\left(\frac{(\Delta V_{IN}) \qquad A_V}{(E_{18} - E_{17})/A_L}\right) \qquad \text{Decibels}$$

where

ΔV_{IN} = the change in input voltage

A_V = voltage gain of the driven amplifier = R_2/R_1

$E_{18} - E_{17}$ = change in output voltage corresponding to ΔV_{IN}

A_L = loop gain for the nulling amplifier circuit = 1000

4.16 Settling Time (ts). Settling time is measured in the circuit of Figure 4. A pulse of specified amplitude and rise time much faster than the settling time of the amplifier in test is applied to the input. The input and output voltages are compared at the output of the FET voltage follower stage using an oscilloscope or alternate apparatus. The ratio of input and feedback resistors, R_1 and R_2, will be specified in the procurement document and will generally be 1 to 1. The scaling factor for the voltage follower input R_3/R_4 may be specified in the procurement document or chosen for convenience in making an accurate measurement. The waveform is observed as illustrated in Figure 4 with δV adjusted for the voltage follower divider ratio if necessary.

Alternate Settling Time Test: Using the circuit shown in Figure 5. A specified input pulse is applied to the device under test. The output waveform is observed on an oscilloscope as illustrated in Figure 6. V_1 is a specified level and V_2 is the final voltage after settling. The settling time is determined as the time for the output to fall from V_1 and settle within the specified error band (obtained from the procurement document) of V_2.

4.17 Rise Time (TR (t_r), TR (tf). The transient response rise time (and the fall time if appropriate) are measured using the test circuit shown in Figure 5. An input pulse of rise time and amplitude as specified in the procurement document is applied and the output waveform is observed on the oscilloscope. Pulse duration and repetition rate are set to enable easy observation of output waveform. Rise times are measured between the 10% and 90% points on the output waveform as shown in Figure 6.

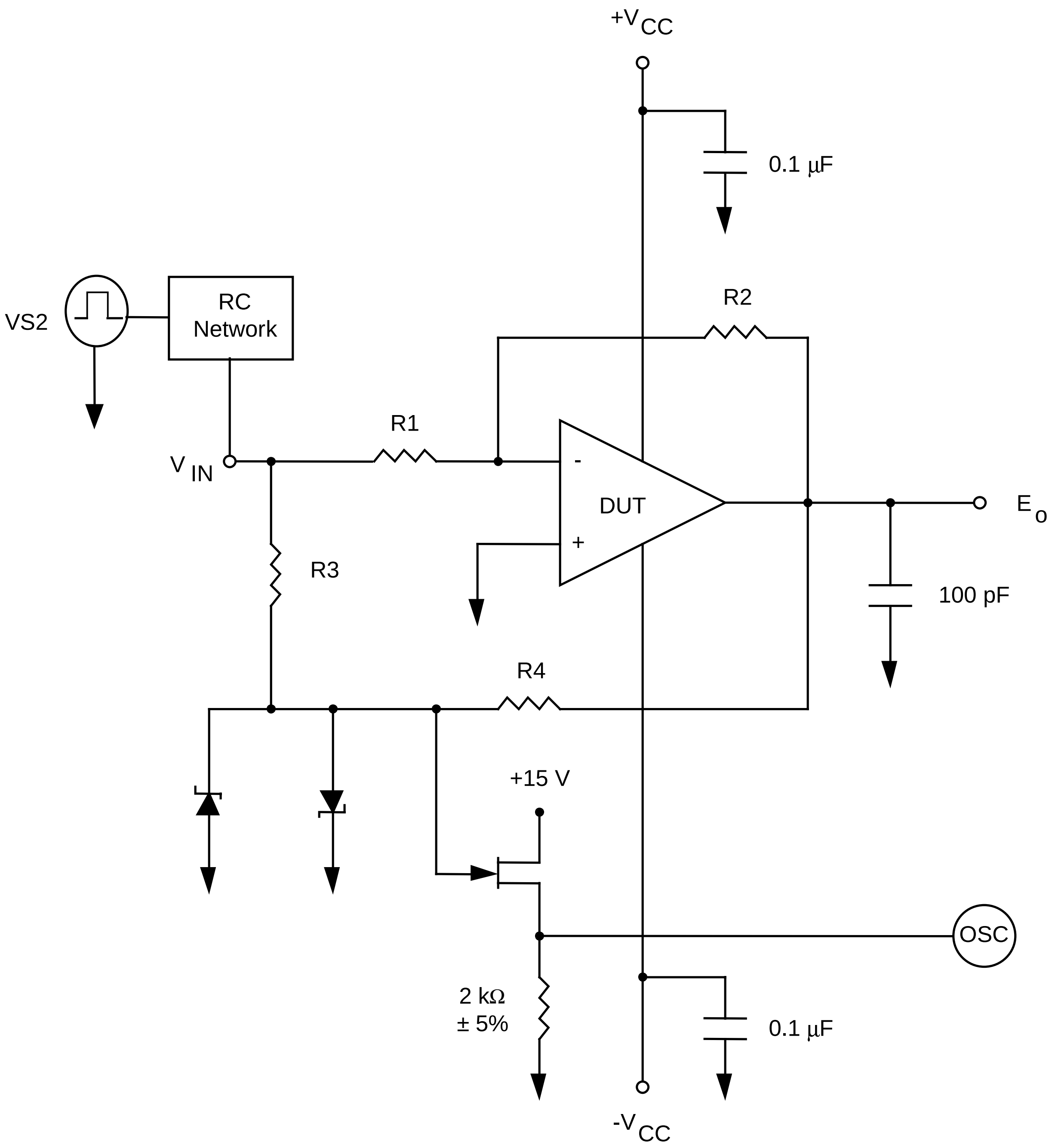
4.18 Slew Rate (SR). Slew rate is also measured using the test circuit in Figure 5. An input pulse of rise time and amplitude as specified in the procurement document is applied to the amplifier. This pulse will cause the output to slew between specified voltages. The output waveform is observed on the oscilloscope and SR(+) and SR(-) calculated for rising and falling waveforms as indicated in Figure 6.

4.19 Broadband Noise ($NI_{(BB)}$). Broadband noise is measured in the circuit of Figure 7 with switch S1 closed. E_o is measured using a true rms voltmeter. All noise measurements are referred to the input. It is assumed that all noise sources within the amplifier in test are set to zero and that the noise measured at the output is input noise multiplied by the circuit gain.

4.20 Popcorn Noise ($N_{I(PC)}$). Popcorn noise is measured in the circuit of Figure 7 with switch S1 closed. E_o is measured using a peak reading voltmeter or equivalent apparatus. The duration of the measurement and the resistance of resistors R_S will be as specified in the procurement document.

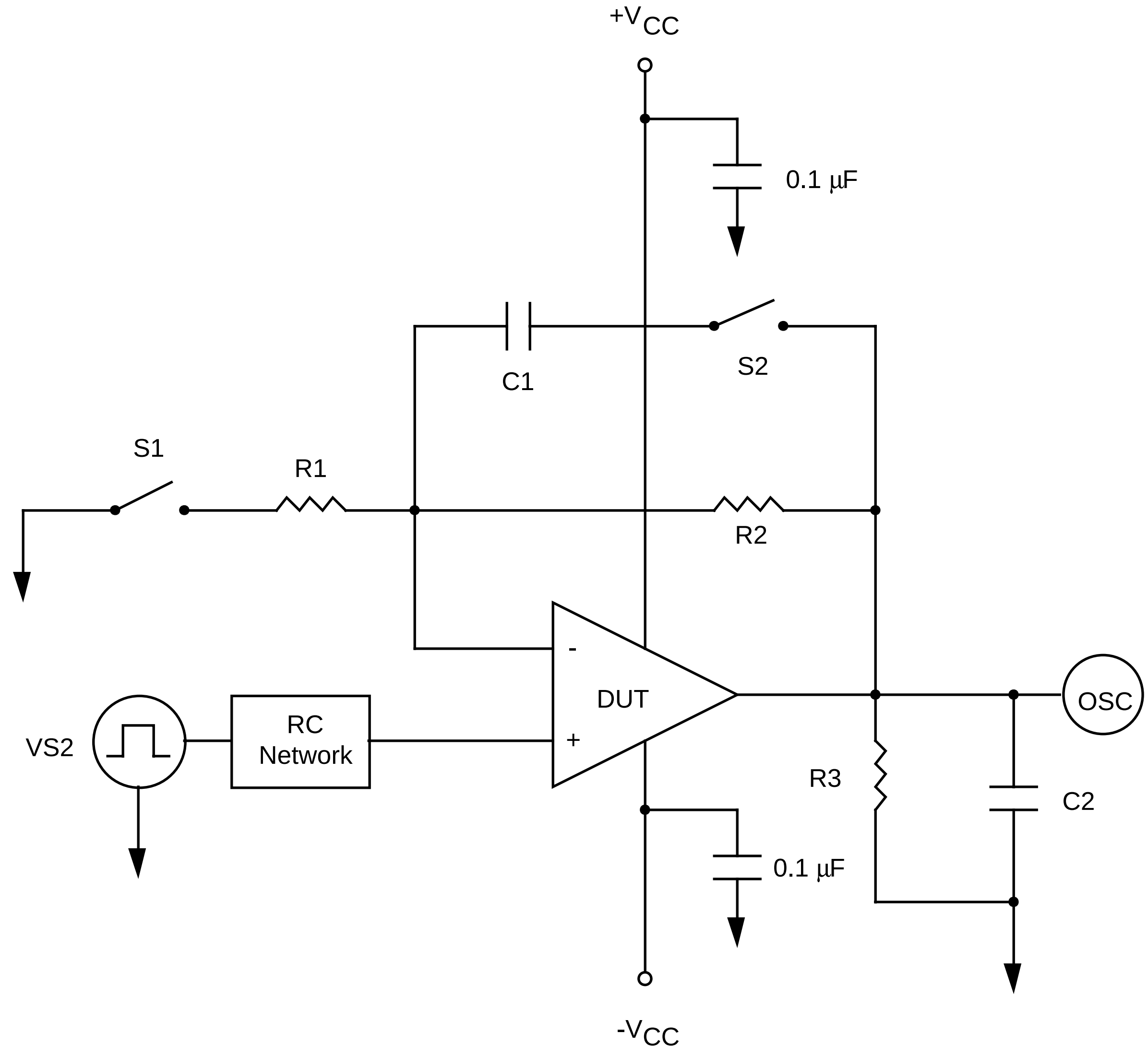
4.21 Input Noise Voltage Density (E_n). E_n is measured in the circuit of Figure 8. The noise analyzer amplifier unit shown is a variable gain low noise amplifier; the noise analyzer filter unit consists of a true rms voltmeter with selectable narrow band input filters. Ideally noise is measured over a 1 Hz bandwidth located at the center of the amplifier bandwidth. This method gives a measured voltage density since the square root of the bandwidth equals 1. In general, the noise analyzer filter unit bandpass filter will have a bandwidth of greater than 1 Hz. To obtain the correct measured noise voltage referenced to the input of the operational amplifier, the voltmeter reading must be corrected for gain and bandwidth.

$$E_m = \frac{E_t}{A\sqrt{NBW}} \qquad V_{RMS}/\sqrt{Hz}$$



Notes:
1. Resistors have ±0.1% tolerance, capacitors have ±10% tolerance unless otherwise specified
2. Precaution shall be taken to prevent damage to DUT during insertion
3. Settling time is the interval during which the summing made is not nulled to within ±0.5ΔV
4. Diodes are 1N5711 Schottky diodes

Figure 4: Operational Amplifier Settling Time Test Circuit



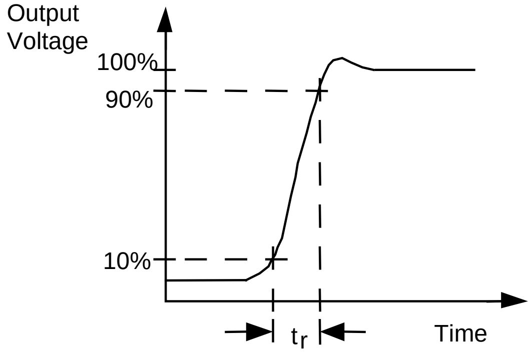
Operational Amplifier Dynamic Parameter Test Circuit

Circuit Gain	Switch S1	Switch S2
Unity	OPEN	CLOSED
R2/R1 + 1	CLOSED	OPEN

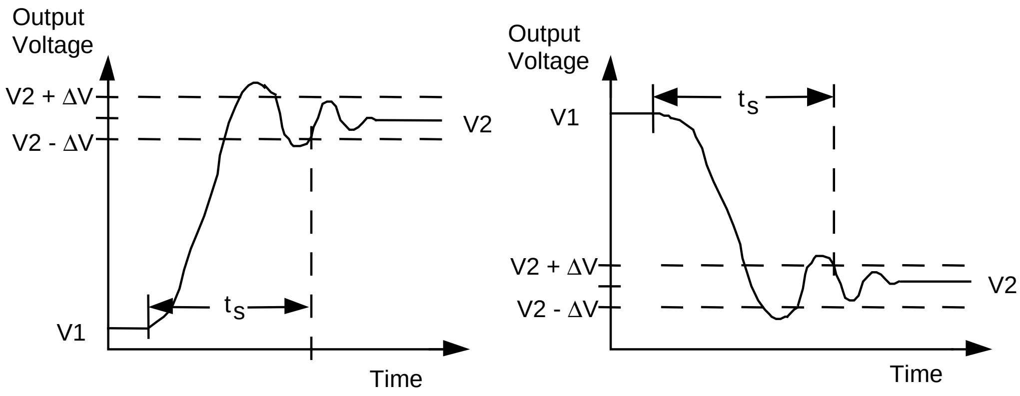
Switch Positions for Dynamic Tests

Note: C1 not required for some part types

Figure 5: Operational Amplifier Dynamic Test Circuit



Rise Time (tr) Waveform

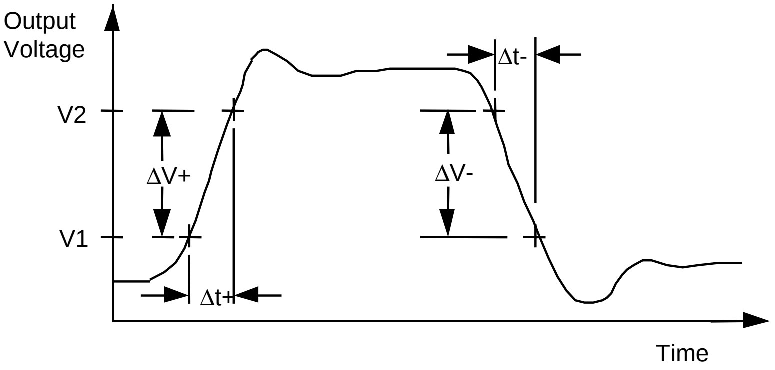


Note: ΔV is allowable error band

Note: ΔV is allowable error band

Settling Time Waveform
For Positive Switching

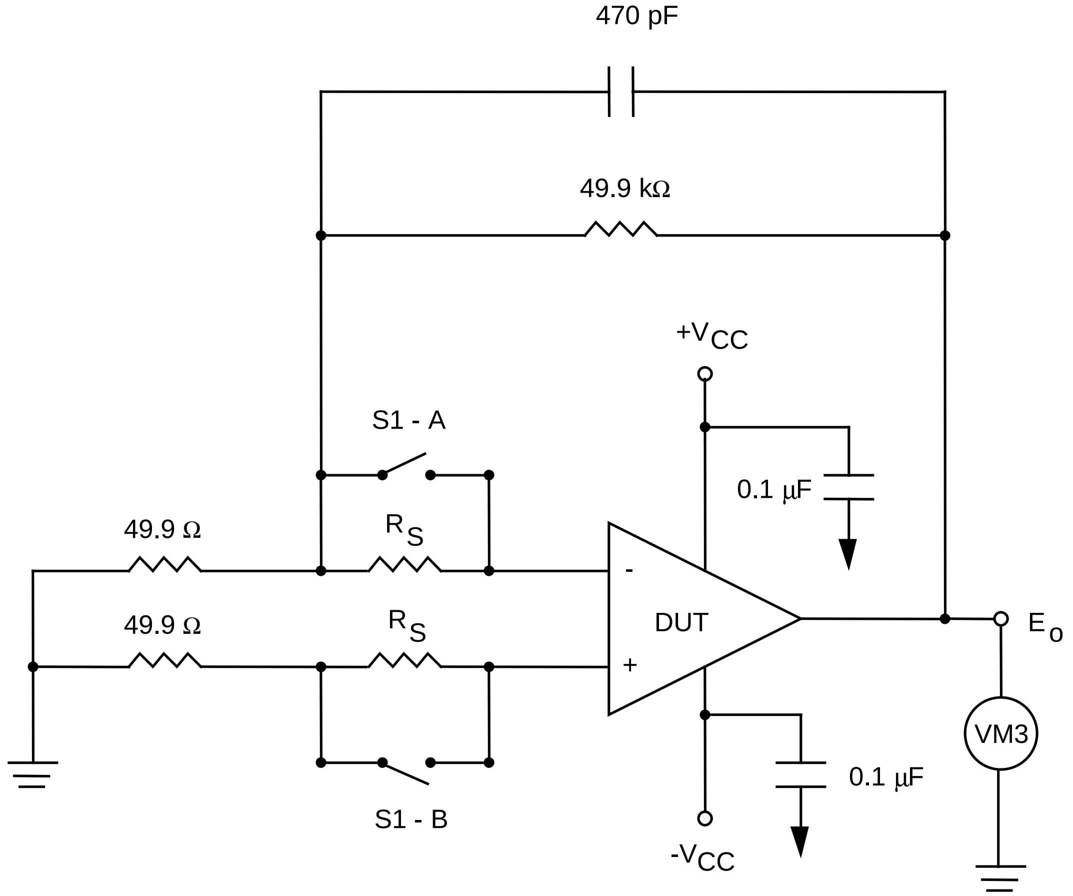
Settling Time Waveform
For Negative Switching



SR(+) = ΔV+/Δt+ SR(-) = ΔV-/Δt-

Slew Rate Waveform

Figure 6: Dynamic Operational Amplifier Test Waveforms



Noise		S1	Measure	Equation	Units
Broadband	$N_{I(BB)}$	Closed	E_o	E_o / 1000	µV rms
Popcorn	$N_{I(PC)}$	Open	E_o	E_o / 1000	µV pk

Notes:
1. R_S = 100 kΩ
2. E_o shall be measured with true rms voltmeter with a bandwidth of 10 Hz to 15 KHz (minimum)
3. The 470 pF capacitor and 49.9 kΩ resistor yield a circuit noise bandwidth of 10 KHz

Figure 7: Noise Test Circuit

where

E_t = rms voltage reading of noise analyzer filter unit

A = total gain of operational amplifier and noise analyzer amplifier unit

NBW = noise bandwidth of bandpass filter at the frequency of measurement

E_m = measured noise voltage density

The square of the measured noise voltage density, E_m , is the sum of the squares of the actual input noise voltage density, the noise voltage density of the input current across the input resistor, and the input resistor thermal noise density.

$$E_m^2 = E_n^2 + R_s^2 * I_n^2 + 4KTR_s$$

where

E_n = input noise voltage density

I_n = input noise current density

4KT = (4)(Boltzman's constant)(°K)

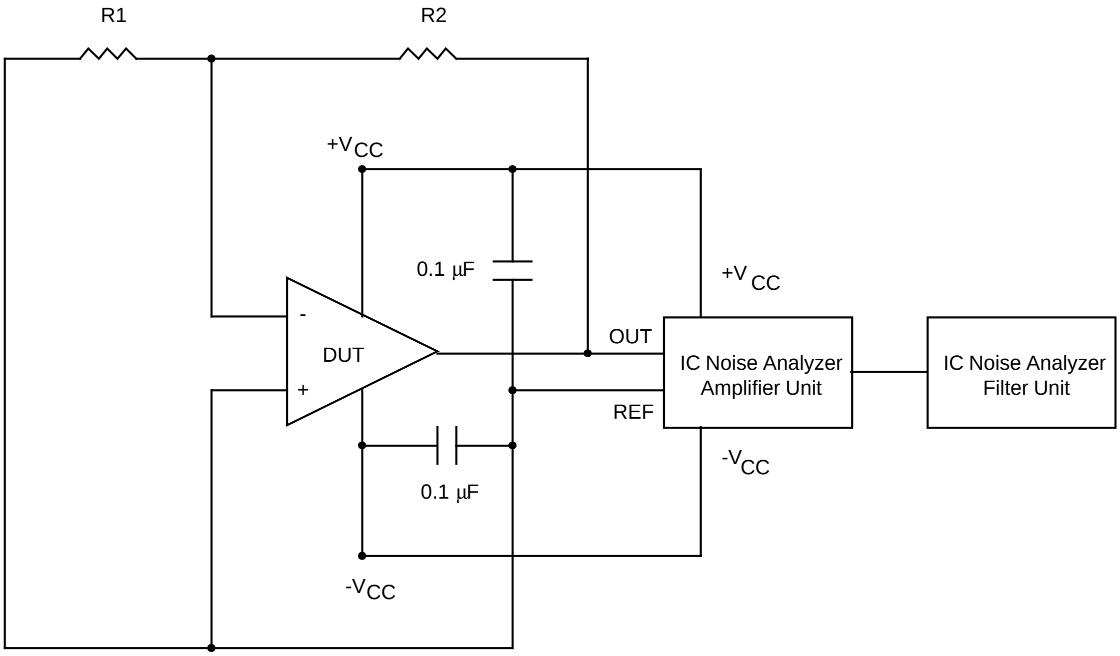
= $1.64 * 10^{-20}$ at 25°C

R_s = source resistance = R_1 in Figure 8

The value of R_S = R_1 of Figure 8 is chosen so that the contribution of the input current density is negligible. Then:

$$E_n^2 = E_m^2 - (1.64 * 10^{-20})\ R_s \qquad (V_{RMS})^2 / \mathrm{Hz}$$

The resistor values R_1 and R_2 may be set in the procurement document. As an example, to obtain E_n , resistors R_1 and R_2 are set to 50Ω and 10 kΩ respectively for an operational amplifier gain of 200. The gain of the noise analyzer amplifier is set to make the total gain to the input of the filter equal to 10,000. The noise voltage, E_t , is measured using the appropriate filter in the noise analyzer filter unit and corrected for amplification and filter bandwidth as above to obtain E_m . E_n is then calculated from E_m using the equation above.



Notes:
1. Input noise voltage density (En) test: R1 = 50Ω, R2 = 10 kΩ
   Input noise current density (ln) test: R1 = 105 kΩ, R2 = 2.0 MΩ
2. All resistors have tolerance of +/- 1%, all capacitors have tolerance of +/- 10%

Figure 8: Noise Density Test Circuit

4.22 Input Noise Current Density (I_n). Noise current density is tested in the circuit of Figure 8 using the same apparatus as for the noise voltage measurement. Noise voltage is first obtained from the procedure of Section 4.21. The measurement is then repeated with the value of resistor $R_1 = R_S$ made large enough that the current contribution to the total noise voltage is significant. Then:

$$I_n^2 = \frac{1}{R_s^2} = \left(E_m^2 - E_n - 1.64 * 10^{-20} * R_s\right)$$

$$I_n = \sqrt{I_n^2} \qquad A/\sqrt{Hz}$$

where all variables are as defined in Section 3.19.

The resistor values R_1 and R_2 may be set in the procurement document. As an example for R_1 = 10 kΩ and R_2 = 2.0 MΩ and gain of the noise analyzer amplifier unit set to give a circuit gain of 10,000 then:

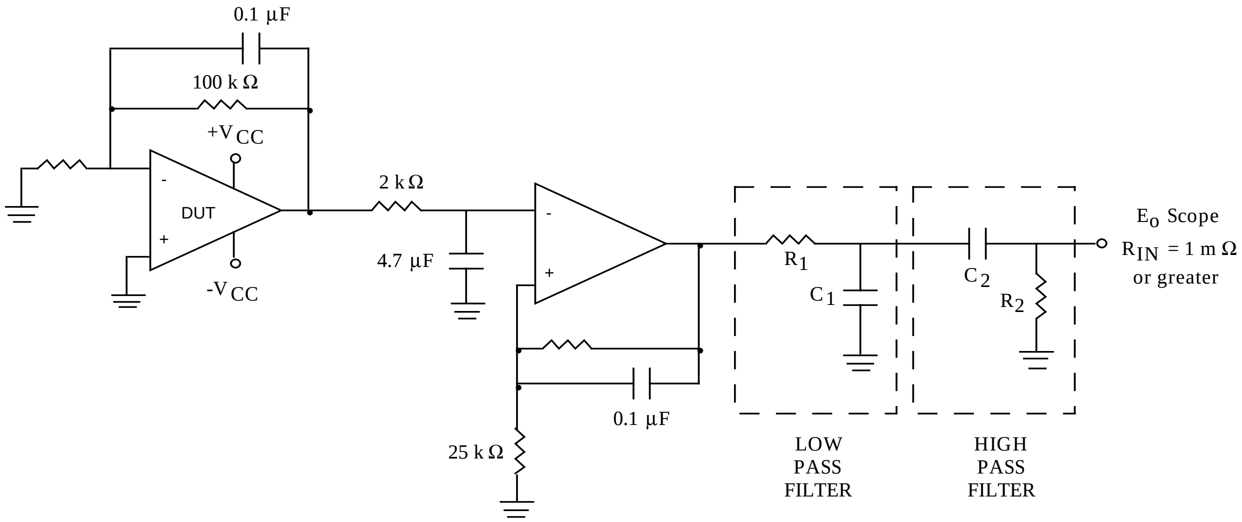
$$I_n^2 = \left(E_m^2 - E_n - 1.64 * 10^{-15}\right) * 10^{-10}$$

$$I_n = \sqrt{I_n^2} \qquad \mathrm{A}/\sqrt{\mathrm{Hz}}$$

where all variables are as defined in Section 4.19.

4.23 Low Frequency Input Noise Density (En_{pp}). Low frequency noise density is tested using the circuit shown in Figure 9. An oscilloscope is used to measure the peak-to-peak output voltage (E_o) of the circuit. Figure 9 illustrates one method of implementing the 0.1 Hz and 10 Hz bandpass filter. The resistor and capacitor values may be set in the procurement document.

$$En_{pp} = \frac{V_o}{\text{Amplifier Gain}} \qquad V_{pp}$$



Notes:
1. The resistor and capacitor values were selected as an example to illustrate the intent of the test.
2. R_1 and C_1 are used to generate the frequency of the low pass filter. R_2 and C_2 are used to generate the 0.1 Hz cutoff frequency of the high pass filter.

Figure 9: Low Frequency Input Noise Density Test Circuit