

1.0 TESTABILITY AND DESIGN - AN INTRODUCTION

1.1 What is Testability?

Testability is the extent to which a system or unit design supports fault detection and fault isolation (FD/FI) within the bounds of specific time, confidence, complexity, and cost effectiveness limits. A system developed using Design for Testability (DFT) criteria will provide the necessary test points to facilitate the incorporation of Built-In-Test (BIT) and support Automated/External Test Equipment (ATE/ETE) while meeting FD/FI requirements. Testability by design will achieve the required FD/FI goals and help to meet Operational Availability (Ao) within complexity and cost constraints. A design methodology utilizing DFT techniques to achieve a high level of testability must be considered early in the design phase.

The goal of testability by design is to assure that all levels of a system meet the requirements of Controllability, Observability, and Accessibility. Controllability is the ability to externally control the functions of a unit to provide test stimuli, disable clocks or break-up chains and feedback loops. Observability is the ability to observe the functions of a unit through BIT/ETE provided by adequate test points and integrated diagnostics. Accessibility is the ability to access the unit's internal structure depending on mission requirements and limited test point placement.

1.2 What is Design for Testability (DFT)?

DFT is a design process intended to achieve a high level of testability by incorporation, early in the design phase, of the following circuit/module/ equipment/system characteristics:

- Initialization - The ability to initialize a system with external stimuli to the operating characteristics of the system. For digital systems, this includes being able to disable internal clocks.
- Controllability - The ability to control the functions of the system with external test stimuli, including clocks, and the ability to break up chains and feedback loops.

- Observability - The ability to observe the functions of the system through adequate test points (0-100%) using integrated diagnostics, (i.e., BIT/ETE/ATE/Manual test/etc.)
- Accessibility - The ability to have 0-100% access to the unit's internal part structures and partitions, depending on mission requirements and limited test point placement.

The means by which DFT is implemented will require the ability to analyze the above characteristics for a given system to identify where improvements are necessary to provide adequate initialization, controllability, observability and accessibility. The analysis can take several forms depending on the type of system and the testability requirements. There are several tools and methods available to the analyst that will provide the necessary information needed to implement DFT principles. This CRTA will identify and describe the most commonly used tools and will attempt to give some guidance on how they can be used alone or together, as in many instances, one tool or method may not sufficiently address all requirements.

1.3 Design for Testability Objectives

As one may have gathered from the definition of DFT, the goals and objectives of any DFT program are to minimize the costs associated with testing for equipment malfunctions while maximizing system Ao. More specifically, these objectives are met by using DFT techniques to help determine where functional test and condition monitoring are needed to assure Ao requirements, and what strategies (i.e., best mix of BIT/ETE/ATE etc. and optimum test performance sequence) are needed to maximize malfunction detection and isolation and decrease test times. In meeting DFT objectives, the benefits of lower Test Program Set (TPS) development costs and lower system life cycle support costs will more than outweigh the cost of implementation.

1.4 Testability Requirements

One of the keys to understanding DFT is to understand the basic requirements of testability. For DFT to be successful and most cost effective, it must be implemented at the earliest design stages. Early implementation will guarantee that adequate testability

is an inherent part of the hardware design. Late incorporation of DFT usually generates extra costs and is much less effective.

Program management must provide for active representation of testability concerns in all program life cycle phases. This means that testability goals are established and monitored and that a testability program plan is developed and adhered to. Part of the program plan should be to evaluate the testability posture at the end of each development phase, before entering the next acquisition phase. This requires that, testability be tracked and demonstrated such that problems can be identified and corrected in a timely and cost effective manner similar to other assurance disciplines.

Testability and DFT techniques should be applied at all hardware indenture levels and at all maintenance levels whenever possible or practical. To decrease test costs in production phases, testability should be considered in a bottom up approach. The bottom up approach will help to facilitate a top down look at testing and testability that is required for operation and maintenance. The various testability tools described herein can be implemented to facilitate a top down, bottom up or combined approach to testability analysis. It is important to remember that applying DFT at all levels of hardware indenture and maintenance will go a long way in maximizing system Availability while minimizing test resource consumption.

1.5 Effective Testability Design Considerations

While the goals, objectives, and requirements of testability and a DFT program have been introduced, the path that one must take to achieve DFT goals, objectives, and requirements has not. For any DFT effort to be successful, certain characteristics of system design must be considered and, if necessary, modified to meet FD/FI requirements. Below is a list of testability design considerations that must be addressed under any DFT program. Keep in mind that some of the listed characteristics may be specific to a particular system technology.

- Provide for initialization of sequential circuits
- Control oscillator and clock circuits
- Minimize the number of fan-in and fan-out situations
- Minimize ambiguity group sizes

- Design a high % of accessible input and output nodes
- Limit the number of feedback loops
- Eliminate digital race problems
- Generate accurate documentation
- Eliminate excessive or redundant tests
- Eliminate undetectable failures to meet FD requirements

To properly affect the inherent testability of a design, each of the above characteristics needs to be addressed. The available testability tools and techniques that are discussed in this CRTA will provide the means to achieve these objectives.

1.6 Benefits of DFT and Testability Analysis

It is generally accepted that the testability characteristics of a system are the direct result of the design of that system. Providing desirable supportable features that yield acceptable operational readiness and reduced operating and support costs can only result when sound engineering design principles are applied.

Although testability analyses are called for in some system procurements, there is currently no common standard, or handbook, that completely defines the methodology or tools to be used. MIL-STD-2165, "Testability Program for Electronic Systems and Equipment," is a good foundation, as a testability standard, but does not adequately address testability analysis techniques and their applications. This CRTA provides an overview of commonly accepted techniques and focuses on the most widely used methods.

When testability requirements are not addressed during the conceptual phase of system development, or are postponed until after the advanced development phase, the results are poor operational readiness, long maintenance times and high support costs. The maintainability benefits that can be derived by incorporating testability analysis in the system development are:

- A system design that fits the established maintenance concept
- Effective fault detection through the proper allocation of potential test points to BIT, ETE, and manual test

- Efficient test strategy to fault isolate down to the replaceable unit, at each maintenance level
- Manageable ambiguity group sizes at all maintenance levels
- Feedback loop identification at each maintenance level
- Reduced time and cost for acceptance testing and fault isolation
- Decreased RTOK's (Retest OKs), CND's (Cannot Duplicates) and BCS's (Bench Check Serviceables)
- Lower cost and more precise test program sets (TPS's)
- More exact ATE/ETE specifications
- Reduced Life Cycle Cost (LCC)

1.7 MIL-STD-2165, "Testability Program for Electronic Systems and Equipment"

MIL-STD-2165 is a tri-service approved document used by all branches of the military in the specification and acquisition of quality-assured electronic systems and equipment. The current version is the initial release dated January 26, 1985. The preparing activity is:

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Space and Naval Warfare Systems Command
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MIL-STD-2165 is composed of seven testability related "tasks" contained in its nineteen pages. There are also three supporting appendices: Appendix A, "Testability Program Application Guidance," Appendix B, "Inherent Testability Assessment," and Appendix C, "Glossary of Terms." The three appendices contain an additional fifty-five pages. It defines methodology for the incorporation of adequate and cost-effective testability and BIT features into the equipment design. It sets the requirements and establishes

guidelines for assessing the extent to which a system or a unit supports fault detection and fault isolation. Three different types of tasks are addressed: 1) program monitoring and control tasks, 2) design and analysis tasks and 3) test and evaluation tasks. These three types of tasks may be defined as follows:

- 1) Program monitoring and control tasks focus on providing the information essential to the acquisition, operation and support management of the system/equipment. They relate more to the management responsibilities dealing with the program and less to the technical details.
- 2) Design and analysis tasks focus on the establishment of specific requirements, design practices, the prediction and analysis of testability parameters and other related engineering tasks.
- 3) Test and evaluation tasks are those that determine compliance with specified requirements and assess the validity of the previously made predictions.

The following is a listing of the tasks contained in MIL-STD-2165:

- Task 101: Testability Program Planning
- Task 102: Testability Reviews
- Task 103: Testability Data Collection and Analysis Planning
- Task 201: Testability Requirements
- Task 202: Testability Preliminary Design and Analysis
- Task 203: Testability Detail Design and Analysis
- Task 301: Testability Inputs to Maintainability Demonstration