1.0 INTRODUCTION

This handbook describes design techniques that can be used to improve the hardness of electronic equipment to transient electrical overstress (EOS) originating from various sources. Extensive use of semiconductor devices, scaled-down dimensions in integrated circuits, lower power supply voltages, and increased use of digital information systems have accentuated the problem of damage from electrical transients. The cost to manufacturers and users in terms of induced data errors, equipment downtime, high repair bills, replacement costs, retrofits, and field service calls is unacceptable in today's market - hence the need for the problem to be recognized and dealt with effectively. If a costly failure occurs everyone suffers - the designer, the manufacturer, the distributor, and the customer - regardless of the reason for the failure. The final product needs to be reliable and safe, even in the event it is mishandled or misapplied.

Some potential sources of EOS cannot be prevented - lightning is a prime example. The electromagnetic pulse (EMP) produced by a nuclear weapons detonation is, thankfully, less of a threat than in recent years. The pollution of the electrical environment from man-made causes such as switching transients or electromagnetic interference (EMI) is especially severe in shipboard, urban, and industrial settings. Shielding and suppression are the keys to effective design in all these cases.

Transients in test equipment can damage parts but the detection of the damage and determination of the cause are not simple matters. As a result, the need for replacements is often attributed to defective incoming parts or even pilferage by workers.

Electrostatic discharge (ESD), a subset of EOS, is a particularly insidious threat. Workers and users at every level are, more often than not, either unaware of the problem or skeptical of its existence for several reasons. First, ESD voltages sufficient to damage integrated circuits are often lower than the threshold for human sensory perception, 2 kV to 4 kV. Consequently, a person may acquire enough charge to damage a part, yet be unaware that a static discharge has taken place. Secondly, real ESD events are not readily repeatable or subject to experimental control. Thirdly, a static sensitive device may be grossly mishandled and subjected to ordinarily fatal ESD and still survive if the discharge does not occur at sensitive pins. This only reinforces the belief that failures caused by ESD are attributable to other causes. Fourthly, detection of ESD damage is a time-consuming effort calling for sophisticated techniques and equipment. Finally, damage is not necessarily catastrophic, but may result in early field failures - the so-called latent defect or "walking wounded" syndrome.

In accordance with the memo by Secretary of Defense William J. Perry dated 29 June 1994, performance and commercial specifications and standards are to be used in lieu of military specifications and standards unless no practical alternative exists to meet the user's needs. Waivers for the use of military specifications and standard, must be approved by the Milestone Decision Authority (as defined in Part 2 of DoD Instruction 5000.2). Nevertheless, the concept of defining classes of part, assembly, and equipment ESD susceptibility previously spelled out in military standards is still useful, and reinforces the general notion that proper design to enhance reliability and safety is an indispensable goal. Test methods for classifying parts are specified in MIL-STD-750 Method 1020 for discrete semiconductor devices, and in MIL-STD-883 Method 3015 for microcircuits and all other parts. The draft version of MIL-STD-1686C, dated 26 December 1994 classifies parts by voltage ranges for various ESD models, but no longer includes criteria and procedures for ESD testing of assemblies and equipment. Instead, commercial standards and guides are included as part of the document.

This handbook includes background material on sources of electrical overstress and electrostatic discharge transients, characteristics of protection devices, and methods for minimizing the effects of EOS and ESD by proper printed circuit board layout, grounding and shielding, and use of protective devices. An extensive bibliography is provided for more in-depth reference to the wide range of topics.